Amendments to the Specification:

Please replace the paragraph of page 5, line 10 through page 6, line 2 with the following amended paragraph:

FIG. 2A shows a layout of an embodiment of a semiconductor device having an SOI structure, e.g., an n type transistor having an SOI structure, according to the present invention. FIGS. 2B, 2C, and 2D are each cross-sectional views taken along the lines IIB - IIB', IIC - IIC', and IID - IID', respectively, of FIG. 2A. Referring to FIGS. 2A through 2D, an insulating layer 110 is formed on a p^- type semiconductor substrate 100. A p^- type insular silicon region 120 is formed of single crystal silicon on the insulating layer 110. An n^+ type source region 130, an n^+ type drain region 140, and a p^- type body region 150 are formed in the p^- type insular silicon region 120. The p^- type body region 150 is in an insular state, and a channel may be formed thereon. A p^+ body contact region 160 is formed next to the n^+ type source region 130 and the p^- type body region 150. In other words, the p^+ type body contact region 160 contacts one side of the n^+ type source region 130 and one end of the p^- type body region 150. A conductive layer, i.e., a salicide layer 170, is formed on the p^+ type body contact region 160 and the n^+ type source region 130. The salicide layer 170 is formed of cobalt salicide, titanium salicide, or nickel salicide. Trench isolation layers 180 are formed on the insulating layer 110 in regions where the p^- type insular silicon region 120 and the p^+ type body contact region 160 are not formed. A gate insulating layer 190 and a gate conductive layer 200 are sequentially formed on the p^- type body region 150. The n^+ type source region 130 is connected to a source electrode 210 via a source contact 130c on the salicide layer 170, and the n^+ type drain region 140 is connected to a drain electrode 220 via the salicide layer 170 and a drain contact 140c. The source region 130 and drain region 140 may have a symmetrical structure, i.e., they may be of approximately equal size and may be proportioned symmetrically about the insular body region 150. The gate conductive layer 200 is connected to a gate electrode 230 via the salicide layer 170 and a gate contact 200c. An interlayer dielectric layer 240 insulates electrodes from each other.